

Serial No. 10/749,271  
Amendment dated August 21, 2006  
Office Action dated April 20, 2006

### **AMENDMENTS TO THE CLAIMS**

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Original) An adaptive replay system comprising:  
a staging unit to forward an instruction in a replay loop parallel to an execution unit;  
a selector device coupled to said staging area to place said instruction in an optimal position within said replay loop; and  
a scoreboard coupled to said selector device to store status information for said instruction.
2. (Original) The system of claim 1 wherein said staging unit is comprised of multiple stages.
3. (Original) The system of claim 1 wherein said status information is latency, dependency and resource conflict information.
4. (Original) The system of claim 2 wherein said multiple stages are equivalent in number to a number of stages in said execution unit.
5. (Original) The system of claim 2 wherein said adaptive replay system is implemented within a multiple channel processor.
6. (Original) The system of claim 5 wherein said selector device is to place said instruction in said optimal position within said replay loop, from a first channel to a second channel, based on status information for said instruction stored in said scoreboard.

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7. (Original) The system of claim 1 wherein said selector device is to analyze at least one instruction per clock cycle to determine whether said at least one instruction has executed correctly.
8. (Original) The system of claim 7 wherein said selector device analyzes 3 instructions per clock cycle.
9. (Original) The system of claim 1 wherein said selector device places said instruction in said optimal position within said replay loop based on status information for said instruction stored in said scoreboard.
10. (Original) The system of claim 9 wherein said selector device can move instructions at least one position relative to a current position to said optimal position in said replay loop.
11. (Original) The system of claim 3 wherein said scoreboard stores latency and dependency information for said instruction when said instruction is first scheduled, and updates latency and dependency information for said instruction when said instruction is executed.
12. (Original) The system of claim 3 wherein said scoreboard stores resource conflicts for said instruction when said instruction encounters a resource conflict during execution.
13. (Original) A computer processing system comprising:  
a multiplexer having a first input, a second input, and an output;

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a scheduler coupled to said multiplexer first input;

an execution unit coupled to said multiplexer output;

a memory device coupled to said execution unit; and

a replay system having an output coupled to said second multiplexer input;

wherein said replay system includes:

a staging unit coupled to said multiplexer output to forward an instruction in a replay loop

parallel to an execution unit; and

a selector device coupled to said staging unit, said selector multiplexer is adapted to place an instruction to an optimal position within said replay loop; and

a scoreboard coupled to said selector device to store status information for said instruction.

14. (Original) The system of claim 13 wherein said staging unit is comprised of multiple stages.

15. (Original) The system of claim 13 wherein said status information is latency, dependency and resource conflict information.

16. (Original) The system of claim 14 wherein said replay system is implemented within a multiple channel processor.

17. (Original) The system of claim 16 wherein said selector device is to place said instruction in said optimal position within said replay loop, from a first channel to a second channel, based on status information for said instruction stored in said scoreboard.

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18. (Original) The system of claim 13 wherein said selector device is to analyze at least one instruction per clock cycle to determine whether said at least one instruction has executed correctly.
19. (Original) The system of claim 13 wherein said selector device is to place said instruction in said optimal position within said replay loop based on status information for said instruction stored in said scoreboard.
20. (Original) The system of claim 19 wherein said selector device can move instructions at least one position relative to a current position to said optimal position in said replay loop.
21. (Original) The system of claim 15 wherein said scoreboard is to store latency and dependency information for said instruction when said instruction is first scheduled, and updates latency and dependency information for said instruction when said instruction is executed.
22. (Original) The system of claim 15 wherein said scoreboard stores resource conflicts for said instruction when said instruction encounters a resource conflict during execution.
23. (Original) A method of processing a computer instruction in a replay loop comprising:
- analyzing multiple instructions from a staging unit;
  - checking a scoreboard for latency information for each of said multiple instructions;
  - checking said scoreboard for dependency information for each of said multiple instructions;
  - checking said scoreboard for resource conflicts for each of said multiple instructions;

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determining an optimal position for each of said multiple instructions in said replay loop; and  
moving each of said instructions to said optimal position in said replay loop.

24. (Original) The method of claim 23 wherein analyzing multiple instructions from a staging unit, a replay selector device analyzes 3 instructions per clock cycle.

25. (Original) The method of claim 23 wherein determining an optimal position for each of said multiple instructions in said replay loop is based on latency, dependency and resource conflict information for said instruction stored in said scoreboard.

26. (Original) The method of claim 23 wherein moving each of said instructions to said optimal position in said replay loop, a replay selector device can move instructions at least one position relative to a current position to said optimal position in said replay loop.

27. (Original) A set of instructions residing in a storage medium, said set of instructions capable of being executed by a processor to implement a method of processing a computer instruction in a replay loop comprising:

analyzing multiple instructions from a staging unit;

checking a scoreboard for latency information for each of said multiple instructions;

checking said scoreboard for dependency information for each of said multiple instructions;

checking said scoreboard for resource conflicts for each of said multiple instructions;

determining an optimal position for each of said multiple instructions in said replay loop; and

moving each of said instructions to said optimal position in said replay loop.

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28. (Original) The set of instructions of claim 27 wherein analyzing multiple instructions from a staging unit, a replay selector device analyzes 3 instructions per clock cycle.

29. (Original) The set of instructions of claim 27 wherein determining an optimal position for each of said multiple instructions in said replay loop is based on latency, dependency and resource conflict information for said instruction stored in said scoreboard.

30. (Original) The set of instructions of claim 27 wherein moving each of said instructions to said optimal position in said replay loop, a replay selector device can move instructions at least one position relative to a current position to said optimal position in said replay loop.